III. In the Claims

Claims 1-30 are pending in the present application. Claims 1-11, 13, 15-19, 21 and 27 have been canceled. Claims 12, 14, 20, 22, 23, 25, 26, 28 and 29 have been amended as set forth below. New Claim 31 has been added. This listing and version of the claims replaces all prior listings and version of the claims.

1-11. (canceled)

12. (currently amended) A semiconductor memory device, comprising:

~~a bit line;~~

~~a plurality of memory cells and a bit switch coupled between said memory cells and a supply voltage node;~~

~~means for detecting a bit line current provided to said memory cells; and~~

a plurality of bit lines coupled to a supply voltage node, each of said bit lines comprising respective plurality of memory cells coupled to said supply voltage node through a respective bit switch, wherein a group of said memory cells are addressable together for programming or overerase correction;

means for adjusting a supply voltage at said supply voltage node responsive to a detection of a total bit line current provided to said plurality of bit lines ~~said detected bit line current~~ to at least partially compensate for a voltage drop across said bit switches, said voltage drop being dependent at least in part on said total bit line current, said adjustment comprising increasing said supply voltage responsive to a detected increase in said total bit line current and decreasing said supply voltage responsive to a detected decrease in said total bit line current, wherein said adjusting means comprises:

a differential amplifier having an output coupled to said supply voltage node; and

a reference voltage generating circuit having an output coupled to a reference voltage input of said differential amplifier, said reference voltage generating circuit comprising a resistance circuit coupled to a current mirror circuit, said current mirror circuit configured to mirror said total bit line current with a reduction ratio.

13. (canceled)

14. (currently amended) The semiconductor device of claim 12, wherein said ~~further comprising means for~~ adjusting means ~~said supply voltage to~~ maintains a bit line voltage at a ~~said~~ memory cell from said plurality of memory cells that is substantially constant during programming or overerase correction ~~of said cell~~.

15-19. (canceled)

20. (currently amended) A ~~The~~ semiconductor memory device, comprising: ~~of claim 15,~~

a plurality of bit lines coupled to a supply voltage node, each of said bit lines comprising respective plurality of memory cells coupled to said supply voltage node through a respective bit switch, wherein a group of said memory cells are addressable together for programming or overerase correction;

means for detecting a total bit line current provided to said plurality of bit lines;

means for adjusting said supply voltage responsive to said detected total bit line current to at least partially compensate for a voltage drop across said bit switches, said voltage drop being dependent at least in part on said total bit line current,

wherein said supply voltage comprises a fixed reference voltage component and variable voltage component responsive to said detected total bit line current,

said semiconductor device further comprising means for incrementally adjusting a relationship between said variable component and said total bit line current in response to respective memory cells from said group of memory cells reaching a programmed state,

wherein said adjusting means comprises a reference voltage generating circuit comprising a tunable resistance circuit coupled to a current mirror circuit, said current mirror circuit configured to mirror said total bit line current with a reduction ratio.

21. (canceled)

22. (currently amended) The semiconductor device of claim 20 ~~21~~, further comprising means for adjusting a resistance of said tunable resistance circuit responsive to a plurality of control signals indicative of whether each of said respective cells from said group of memory cells is in a programmed state.

23 (currently amended) The semiconductor device of claim 22, wherein said relationship ~~amount~~ is adjusted after each respective cell from said group of memory cells reaches said programmed state.

24. (original) The semiconductor device of claim 20, further comprising means for generating said variable voltage component.

25. (currently amended) The semiconductor memory device of claim 12 ~~15~~, wherein said semiconductor memory device is a flash memory device comprising flash memory cells organized in an array of I/O blocks, each I/O block comprising a plurality of columns and plurality of rows, said array of I/O blocks comprising said plurality of bit lines.

26. (currently amended) A semiconductor memory device comprising flash memory cells organized in an array comprising a plurality of columns and plurality of rows, said plurality of columns comprising a plurality of bit lines each comprising a respective one of the memory cells coupled to a supply voltage through a respective bit switch, wherein a group of said memory cells are addressable together for programming, said semiconductor device further comprising:

means for detecting a total bit line current provided to a plurality of bit lines associated with said group of memory cells;

a regulated supply voltage source for providing said supply voltage, said supply voltage comprising a fixed reference voltage component and a variable voltage component responsive to said detected total bit line current, wherein said supply voltage is adjusted to track changes in total bit line current provided to said plurality of bit lines associated with said group; and

means for adjusting, in response to respective memory cells reaching a programmed state, a relationship between said variable voltage component and said total bit line current, said adjusting means comprising a reference voltage generating circuit comprising a tunable resistance circuit coupled to a current mirror circuit, said current mirror circuit configured to mirror said total bit line current with a reduction ratio.

27. (canceled)

28. (currently amended) The semiconductor device of claim 26 ~~27~~, further comprising means for adjusting a resistance of said tunable resistance circuit responsive to a control signal indicative of whether each of said respective cells are in a programmed state.

29 (currently amended) The semiconductor device of claim 28, wherein said relationship ~~amount~~ is adjusted after each respective cell reaches said programmed state.

30. (original) A semiconductor memory device, comprising:

a bit line;

a memory cell and a bit switch coupled between said memory cell and a supply voltage node;

a current mirror circuit configured to mirror a bit line current through said memory cell with a reduction ratio;

a voltage source having an output coupled to said supply voltage node and responsive to a reference voltage; and

a reference voltage generator circuit having an output coupled to a reference voltage input of said voltage source, said reference voltage generator circuit comprising a resistance circuit coupled to said current mirror circuit,

wherein said reference voltage generator circuit provides a reference voltage for said voltage source that is responsive to said mirrored bit line current,

whereby said supply voltage at said supply voltage node is adjusted responsive to said bit line current to at least partially compensate for a voltage drop across said bit switch, said voltage drop being dependent at least in part on said bit line current.

31. (new) The semiconductor memory device of claim 20, wherein said semiconductor memory device is a flash memory device comprising flash memory cells organized in an array of I/O blocks, each I/O block comprising a plurality of columns and plurality of rows, said array of I/O blocks comprising said plurality of bit lines.